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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	
	Filing Date	10/530298
	First Named Inventor	Andrei Radulescu
	Art Unit	4144
	Examiner Name	Nishant Divecha
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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number No.-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
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FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number No.-no.-kind ² , if known	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited document	Pages, Columns Lines, Where Relevant Passages or Relevant Figures Appear
/N.D./		WO 02 23814	03-21-2002	SUN MICROSYSTEMS	

NON-PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. ¹	Include name of the author (in capital letters), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ⁴
/N.D./		S KUMAR ET AL: "A NETWORK ON CHIP ARCHITECTURE AND DESIGN METHODOLOGY"			
/N.D./		GUERRIER P ET AL "A GENERIC ARCHITECTURE FOR ON-CHIP PACKET-SWITCHED INTERCONNECTIONS" 27 MARCH 2000, PAGES 250-256			
/N.D./		MOON SAN-JUN ET AL: "SCALABLE AND RELIABLE ATM MULTICAST EMPLOYING RM CELL CONSOLIDATION" ELECTRONIC LETTERS, IEE STEVENAGE, GB, VOL. 35, NO. 23, 11 NOVEMBER 1999			

Examiner Signature	/Nishant Divecha/	Date Considered	03/20/2008
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